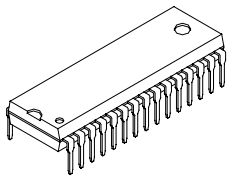
SONY

CXA2066S

Preamplifier for High Resolution Computer Display

30 pin SDIP (Plastic)



Description

The CXA2066S is a bipolar IC developed for high resolution computer displays.

Features

- Built-in wide band amplifier: 140MHz @ –3dB (Typ.)
- Input dynamic range: 1.0Vp-p (Typ.)
- High gain preamplifier (17dB)
- R, G, and B incorporated in a single package
- I^2C bus control
  - Contrast control
  - Subcontrast control
  - Brightness control
  - OSD contrast control
  - Cutoff control 4-channel DAC output
  - 2 blanking level modes (0.5V fixed and Pedestal –0.6V)
  - ABL control pin
- Built-in sync separator for Sync on Green
- Built-in blanking mixing function
- Built-in OSD mixing function
- Video period detection function
- Built-in sharpness function
- Built-in VBLK synchronous DAC refresh system

Applications

High resolution computer displays

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

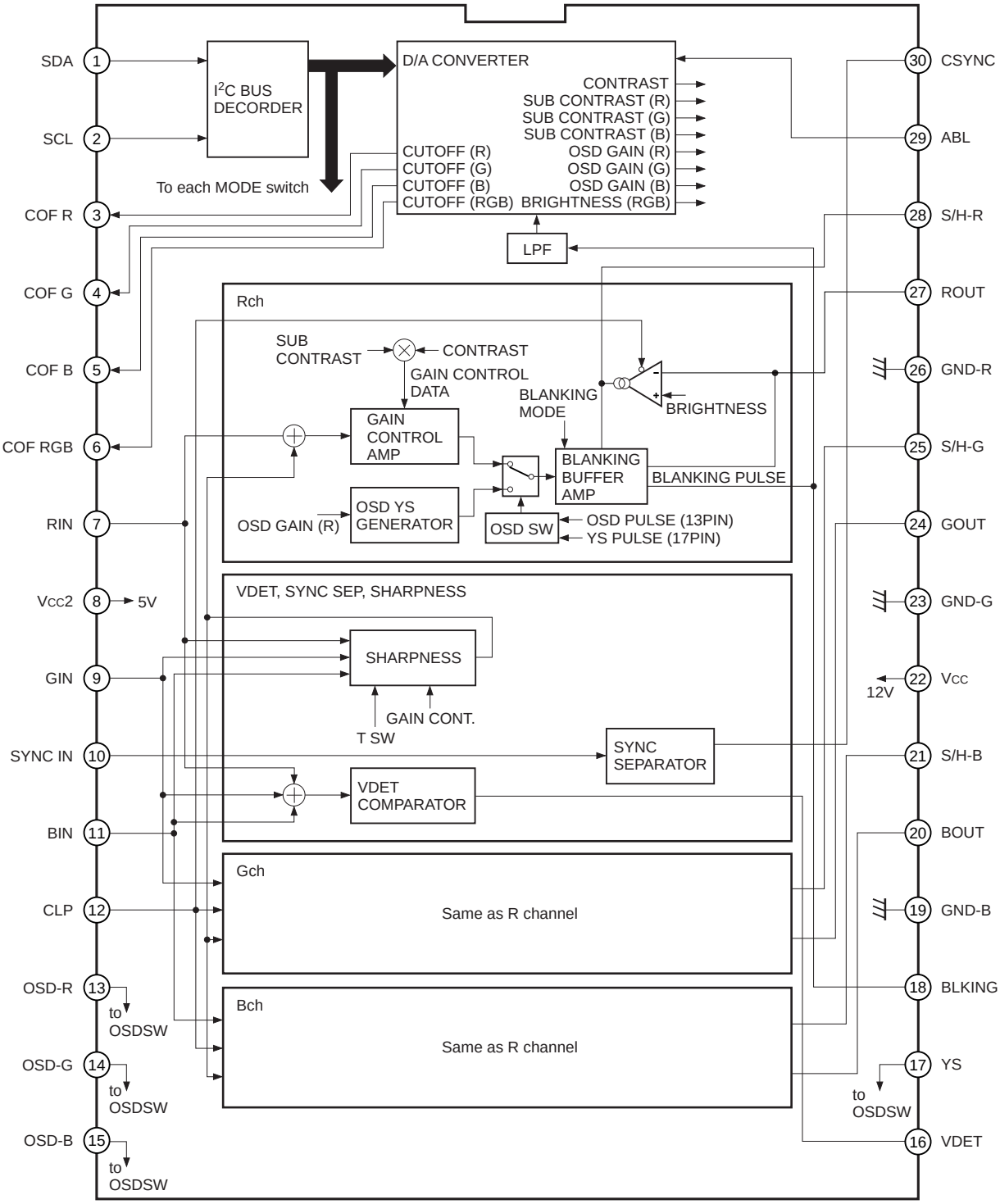
• Supply voltage	V_{CC}	14	V
	$V_{CC}2$	7	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	2.05	W

Recommended Operating Conditions

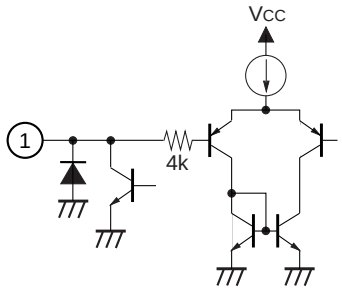
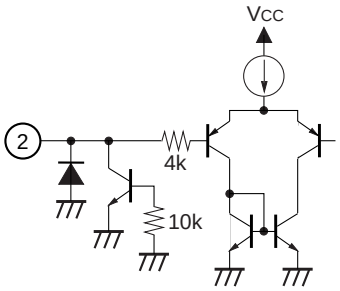
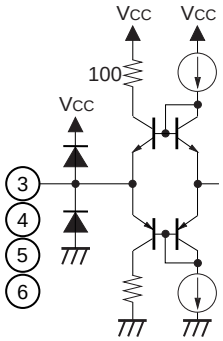
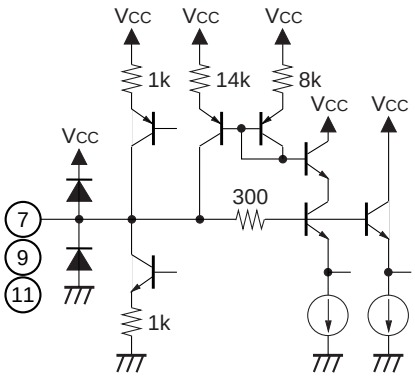
Supply voltage	V_{CC}	12 ± 0.5	V
	$V_{CC}2$	5 ± 0.5	V

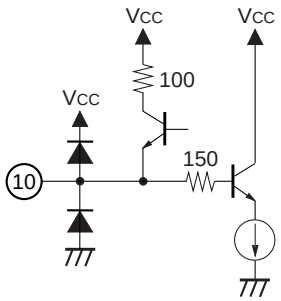
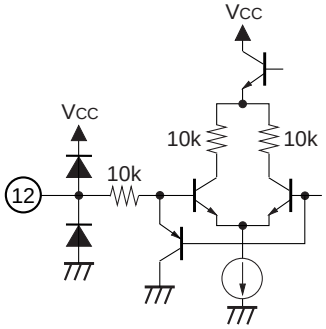
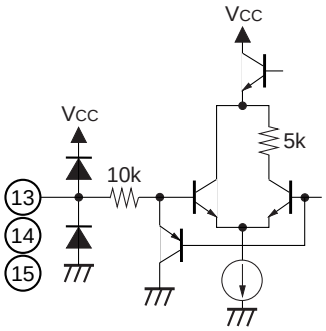
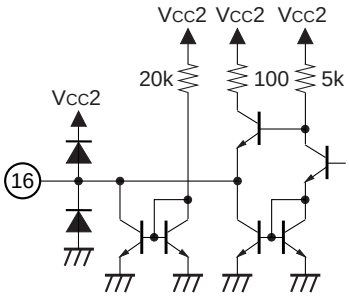
E98210-PS

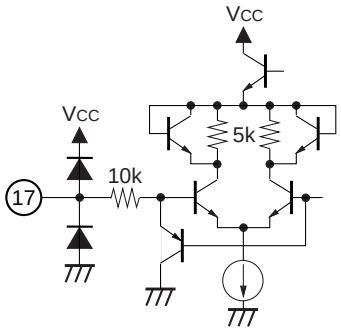
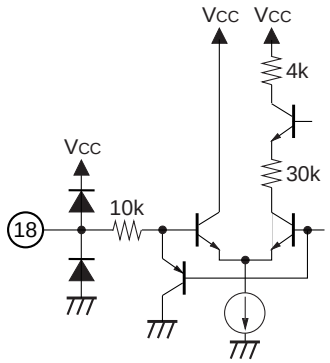
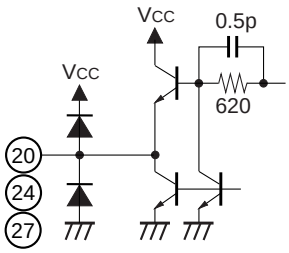
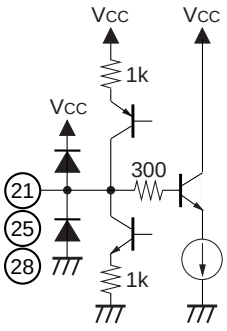
Block Diagram

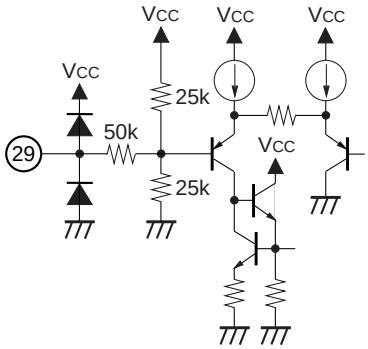
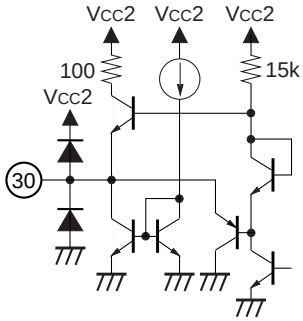


Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	SDA			I²C bus standard SDA (serial data) input/output. VILMAX = 1.5V VIHMIN = 3.5V VOLMAX = 0.4V
2	SCL			I²C bus standard SCL (serial clock) input. VILMAX = 1.5V VIHMIN = 3.5V
3 4 5 6	COF R COF G COF B COF RGB			Cut-off adjustment DAC outputs. The output DC is 1 to 4V.
7 9 11	RIN GIN BIN	1.7V (when clamped)		RGB signal inputs. Input via the capacitor.
8	Vcc2	5V		5V power supply.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
10	SYNC IN	2.8V		Sync on Green signal input. Input via the capacitor.
12	CLP			Clamp pulse (positive polarity) input. VILMAX = 0.8V VIHMIN = 2.8V
13 14 15	OSD-R OSD-G OSD-B			OSD control inputs. VILMAX = 0.8V VIHMIN = 2.8V
16	VDET			Video detector output. Typ.; High = 4.3V Low = 0.2V

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
17	YS			YS (OSD_BLK) input. VILMAX = 0.8V VIHMIN = 2.8V
18	BLKING			Blanking pulse input. Set the V blanking pulse width to 300µs or more. VILMAX = 0.8V VIHMIN = 2.8V
19 23 26	GND-B GND-G GND-R	0V		GNDs.
20 24 27	BOUT GOUT ROUT			R, G, and B signal outputs.
21 25 28	S/H-B S/H-G S/H-R			Brightness sample-and-hold. Connect a capacitor to GND.
22	Vcc	12V		12V power supply.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
29	ABL			ABL control input. Ground to GND when not using ABL.
30	CSYNC			Sync on Green signal sync separator output (positive polarity). Typ.; High = 4.3V Low = 0.2V

I²C BUS Register Definitions

Slave Address

SLAVE RECEIVER; 40 (HEX)

Register Table

SUB ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	CONTRAST							
01H	0	BLK MODE	BRIGHTNESS					
02H	CUT OFF R							
03H	CUT OFF G							
04H	CUT OFF B							
05H	VDET LEVEL		OSD GAIN					
06H	CUT OFF RGB							
07H	SUB CONTRAST R							
08H	SUB CONTRAST G							
09H	SUB CONTRAST B							
0AH	V DET OFF	SHP OFF	SYNC OFF	T SW	SHP GAIN			

Sub Address 0000 CONTRAST (8)

Controls the gain common to the R, G, and B channels. Since control is performed by multiplying with SUB CONTRAST, the white balance can be adjusted by SUB CONTRAST and the luminance can be adjusted by CONTRAST.

0: Gain minimum (–30dB or less)
255: Gain maximum (+17dB)

Sub Address 0001 BLK MODE (1)

Switches the blanking level.

0: Pedestal –0.6V
1: 0.5V fixed

Sub Address 0001 BRIGHTNESS (6)

Controls the black level common for the R, G, and B channels.

0: Black level minimum (1V)
63: Black level maximum (3V)

Sub Address 0010 CUT OFF R (8)

Controls Pin 3 (COF R) output voltage.

0: Output voltage minimum (1V)
255: Output voltage maximum (4V)

Sub Address 0011 CUT OFF G (8)

Controls Pin 4 (COF G) output voltage.

0: Output voltage minimum (1V)
255: Output voltage maximum (4V)

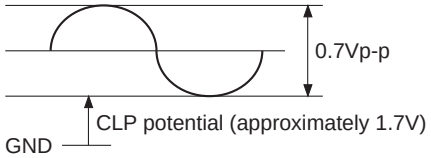
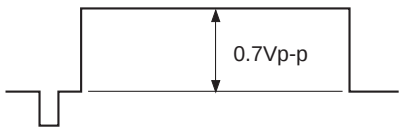
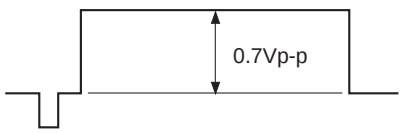
Sub Address 0100 CUT OFF B (8)

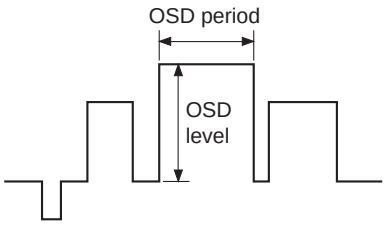
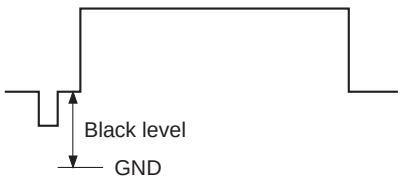
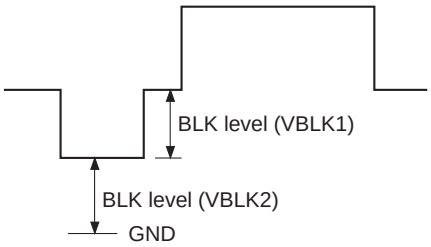
Controls Pin 5 (COF B) output voltage.

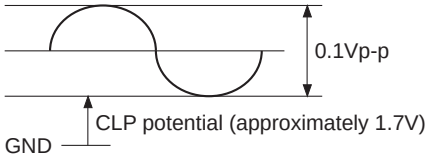
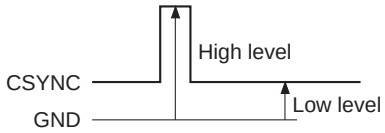
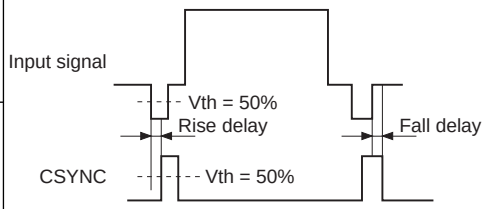
0: Output voltage minimum (1V)
255: Output voltage maximum (4V)

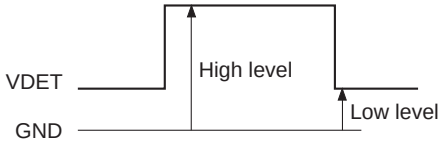
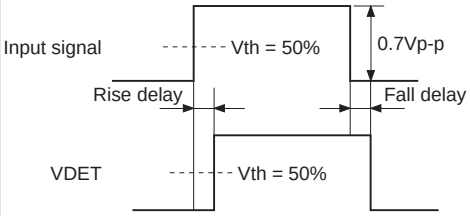
Sub Address 0101	VDET LEVEL (2)	Controls the signal detection (VDET) slice level. 0: Slice level minimum (30mV when RIN = GIN = BIN) 3: Slice level maximum (220mV when RIN = GIN = BIN)
Sub Address 0101	OSD GAIN (6)	Controls the OSD gain common to the R, G, and B channels. Since control is performed by multiplying with SUB CONTRAST (upper 6 bits), white balance and tracking for the video is obtained. 0: Gain minimum (0Vp-p) 63: Gain maximum (5Vp-p)
Sub Address 0110	CUT OFF RGB (8)	Controls Pin 6 (COF RGB) output voltage. 0: Output voltage minimum (1V) 255: Output voltage maximum (4V)
Sub Address 0111	SUB CONTRAST R (8)	Controls the R channel gain. Control is performed by multiplying with CONTRAST. Use for adjusting the white balance. 0: Gain minimum (–30dB or less) 255: Gain maximum (+17dB)
Sub Address 1000	SUB CONTRAST G (8)	Controls the G channel gain. Control is performed by multiplying with CONTRAST. Use for adjusting the white balance. 0: Gain minimum (–30dB or less) 255: Gain maximum (+17dB)
Sub Address 1001	SUB CONTRAST B (8)	Controls the B channel gain. Control is performed by multiplying with CONTRAST. Use for adjusting the white balance. 0: Gain minimum (–30dB or less) 255: Gain maximum (+17dB)
Sub Address 1010	VDET OFF (1)	Controls the Pin 16 (VDET) output. 0: VDET output on 1: VDET output off
Sub Address 1010	SHP OFF (1)	Controls the sharpness function. 0: Sharpness on 1: Sharpness off
Sub Address 1010	SYNC OFF (1)	Controls the Pin 30 (CSYNC) output. 0: SYNC output on 1: SYNC output off
Sub Address 1010	T SW (1)	Controls the time constant during sharpness. 0: 50ns 1: 100ns
Sub Address 1010	SHP GAIN (4)	Controls the sharpness gain. 0: Gain minimum (–30dB or less) 15: Gain maximum (+7dB)

Electrical Characteristics

No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption	$I_{CC}1$	V_{CC} and $V_{CC}2$ pins inflow current Input signal: None	65	88	110	mA
		$I_{CC}2$		30	45	60	mA
2	Frequency response (50MHz)	F4	Input continuous 1MHz, 50MHz, and 100MHz sine waves at 0.7Vp-p. Measure the output amplitude gain difference at this time. Gain difference [dB] = 20 log $\left(\frac{V_{OUT}\ 50M}{V_{OUT}\ 1M}\right)$ Gain difference [dB] = 20 log $\left(\frac{V_{OUT}\ 100M}{V_{OUT}\ 1M}\right)$	–1.7	0	1.7	dB
	Frequency response (100MHz)	F5	RGB input signal (RGB input pins) 	–5.5	–1.85	1.8	
3	Contrast control 1	GCONT1	Measure the level of the output signal amplitude V_{OUT} when a 0.7Vp-p video signal is input. (ABL = 0V) VCONT1: Contrast = Sub Contrast = FF VCONT2: Contrast = 00/Sub Contrast = FF	4.5	5.0	5.5	Vp-p
	Contrast control 2	GCONT2	Input signal 	–30	35	100	mVp-p
4	Sub Contrast control	GSUB	Measure the level of the output signal amplitude V_{OUT} when a 0.7Vp-p video signal is input. (Contrast = FF/Sub Contrast = 00/ ABL = 0V) Input signal 	–30	35	100	mVp-p

No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
5	OSD gain control	GOSD1	Measure the OSD level of the output signal when an OSD pulse is input. GOSD1: OSD = 3F/Sub Contrast = FF GOSD2: OSD = 00/Sub Contrast = FF RGB output signal  	4.4	5.0	5.6	Vp-p
		GOSD2		–240	–70	80	mVp-p
6	Brightness control	VBRT1	Measure the black level of the RGB output signal. VBRT1: Brightness = 00 VBRT2: Brightness = 3F RGB output signal  	0.8	1.1	1.4	V
		VBRT2		2.65	2.9	3.15	
7	BLK control (BLK MODE = 0)	VBLK1	Measure the BLK level of the output signal when a BLK pulse is input.  	400	560	720	mV
	BLK control (BLK MODE = 1)	VBLK2		200	310	420	

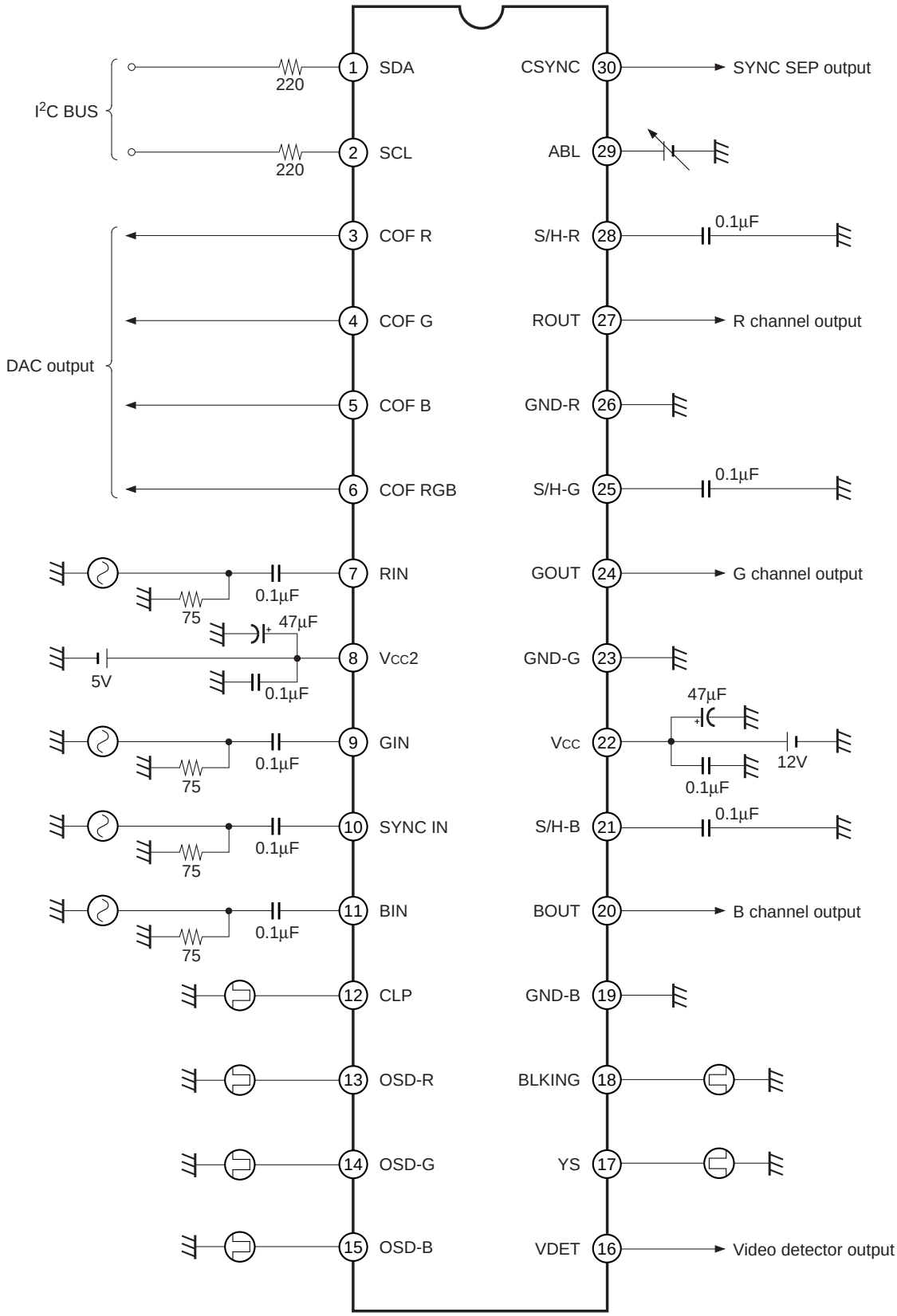
No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
8	Sharpness gain 1	SHP1	Input a 30MHz sine wave to RGB at an amplitude of 0.1Vp-p, and measure the output level, and then calculate I/O gain. Gain difference [dB] = 20 log (Output level / Input level) (Contrast = 7F/Sub Contrast = FF/ ABL = 0V) SHP1: SHP GAIN = 0/T SW = 0 SHP2: SHP GAIN = F/T SW = 0 SHP3: SHP GAIN = 0/T SW = 1 SHP4: SHP GAIN = F/T SW = 0 Input signal 	8.9	10.9	12.9	dB
	Sharpness gain 2	SHP2		14.6	16.6	18.6	
	Sharpness gain 3	SHP3		9.2	11.2	13.2	
	Sharpness gain 4	SHP4		16.3	18.3	20.3	
9	Input D range (VIN = 0.7V)	VIND1	Measure the output level when 0.7Vp-p and 1.2Vp-p input video signals are input. (Contrast = CC, Sub Contrast = FF, Brightness = 00)	3.8	4.3	4.8	Vp-p
	Input D range (VIN = 1.2V)	VIND2		5.8	6.3	6.8	
10	SYNCSEP output high level	SYNCHI	Input a Sync on Green video signal to SYNCIN, and measure the CSYNC high level and low level. 	4.1	4.4	4.7	V
	SYNCSEP output low level	SYNCLO		100	200	300	mV
11	SYNCSEP output rise delay	SDLYR			42	50	ns
	SYNCSEP output fall delay	SDLYF			45	70	

No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
12	VDET output high level	VDETHI	Measure the VDET high level and low level when a 0.7Vp-p video signal is input to RGB. 	4.1	4.4	4.7	V
	VDET output low level	VDETLO		200	280	400	mV
13	VDET output rise delay	VDDLYR			17	40	ns
	VDET output fall delay	VDDLYF			26	50	
14	DAC output voltage (COFF = 00)	VCUT1	Measure the DAC output voltage (Pins 3, 4, 5, and 6) when COFF = 00/FF.	0.9	1.1	1.3	V
	DAC output voltage (COFF = FF)	VCUT2		3.8	4	4.2	

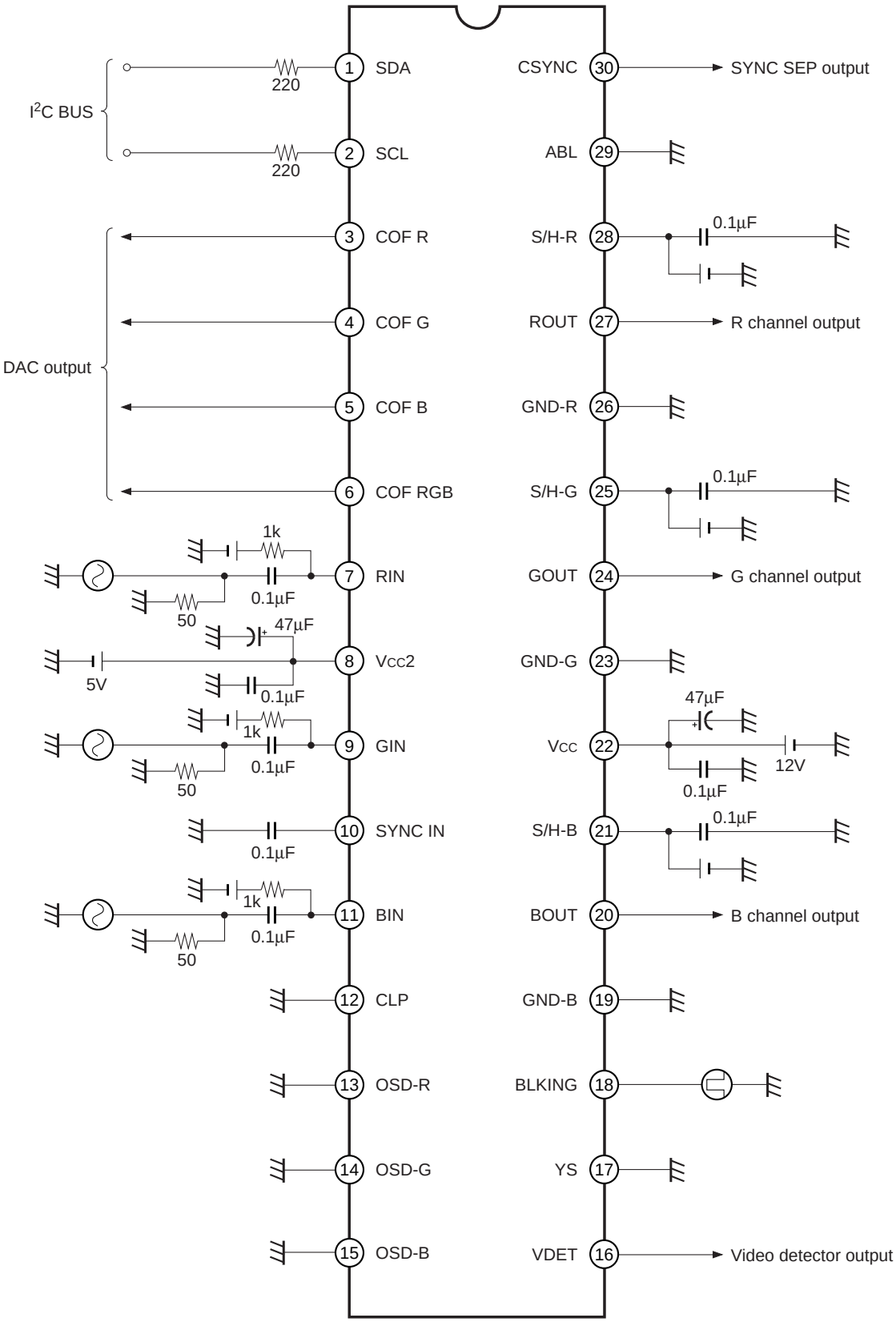
I²C BUS Logic System

No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	V
3	Low level output voltage SDA, during current inflow of 3mA	V_{OL}	0	—	0.4	V
4	Maximum clock frequency	f_{SCL}	0	—	100	kHz
5	Minimum waiting time for data change	t_{BUF}	4.0	—	—	µs
6	Minimum waiting time for data transfer start	t_{HD}; STA	4.0	—	—	µs
7	Low level clock pulse width	t_{LOW}	4.7	—	—	µs
8	High level clock pulse width	t_{HIGH}	4.0	—	—	µs
9	Minimum waiting time for start preparation	t_{SU}; STA	4.7	—	—	µs
10	Minimum data hold time	t_{HD}; DAT	440	—	—	ns
11	Minimum data preparation time	t_{SU}; DAT	250	—	—	ns
12	Rise time	t_R	—	—	1	µs
13	Fall time	t_F	—	—	300	ns
14	Minimum waiting time for stop preparation	t_{SU}; STO	4.7	—	—	µs

Electrical Characteristics Measurement Circuit



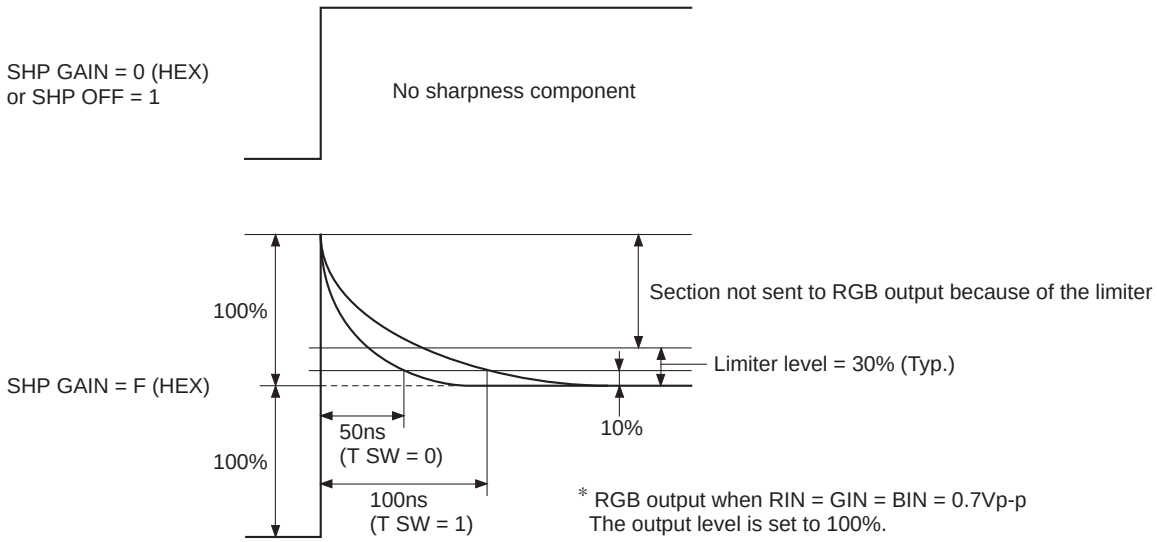
Electrical Characteristics Measurement Circuit (Frequency Response)



Description of Operation

1. Sharpness function

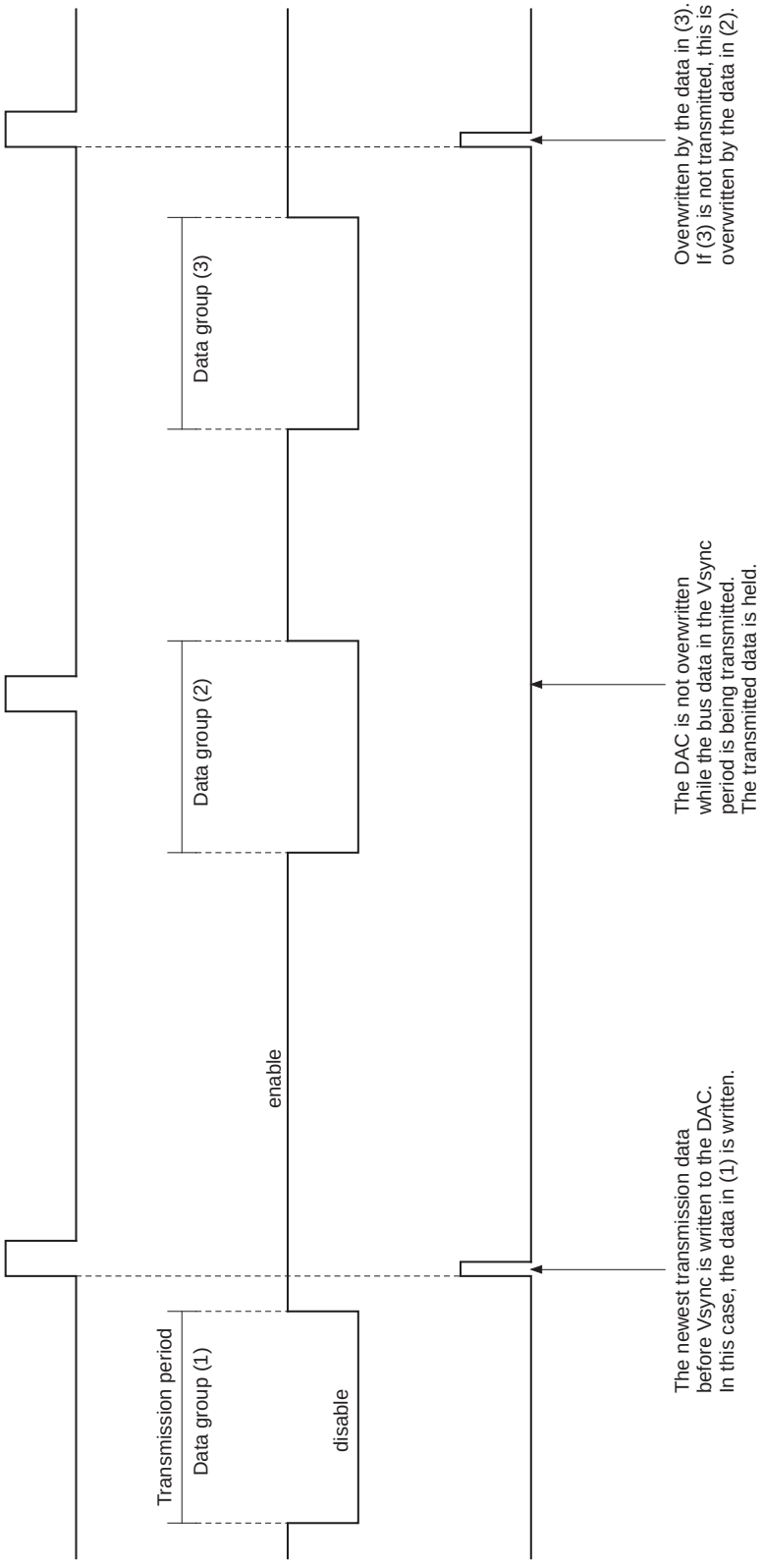
The RGB signals input to Pins 7, 9, and 11 are mixed at a ratio of 0.6G + 0.3R + 0.1B to form the Y signal. The high-frequency component is removed from this Y signal by a differentiation circuit, and the amplitude is controlled by a gain control circuit. The signal which undergoes gain control (sharpness component) has its amplitude clipped by a limiter circuit and is then added to the R, G, and B signals.



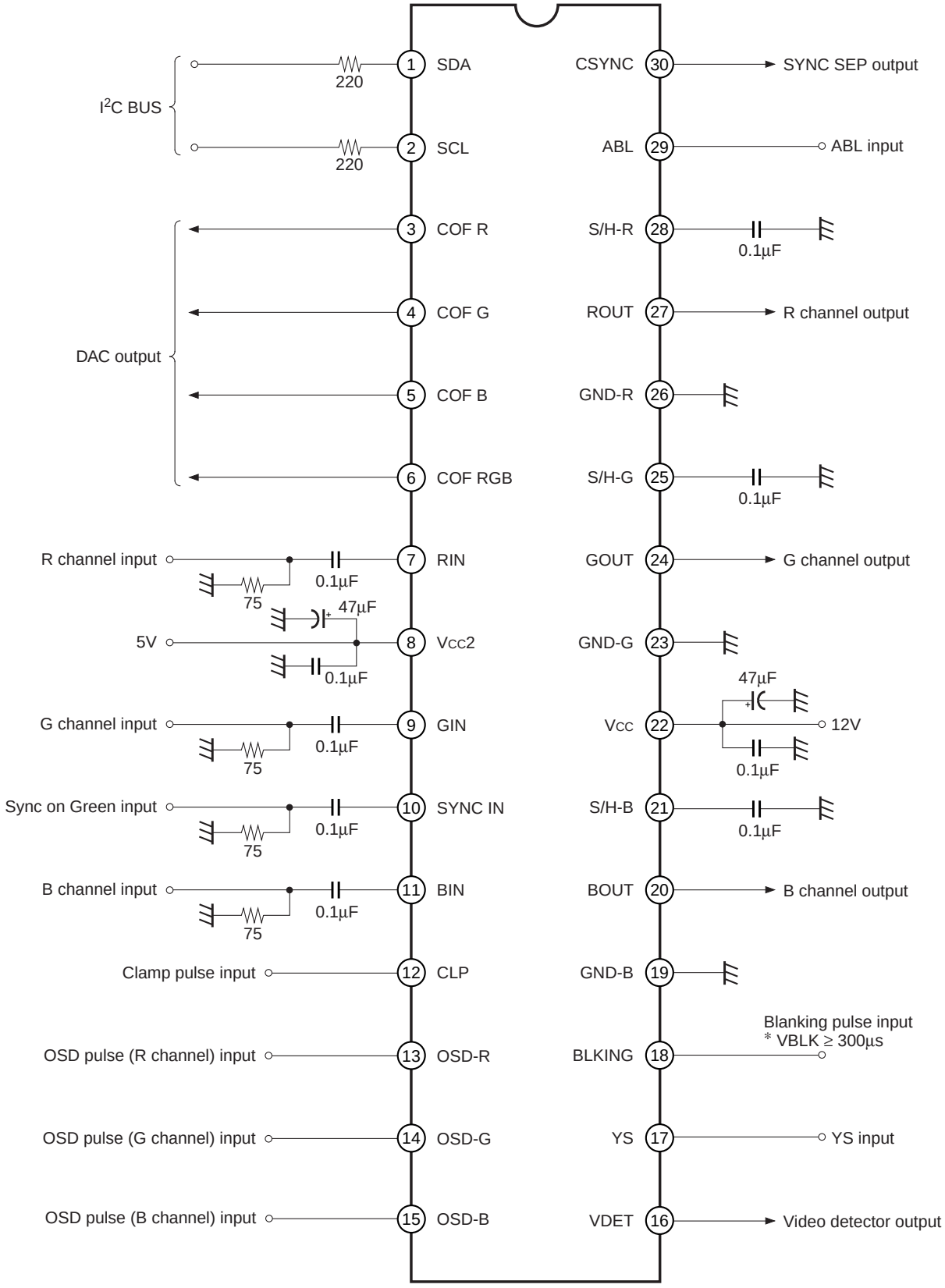
2. VBLK synchronous DAC refresh system

The VBLK signal is removed from the composite BLK signal which has been input to Pin 18, and the data for each control DAC is overwritten all at once in synchronization with this VBLK signal. The received I^2C bus data is held by a latch until the next VBLK signal arrives. As a result, I^2C bus data transmission from the microcomputer is timing-free. Set the V blanking pulse width which is input to Pin 18 at 300µs or more.

VBLK Synchronous DAC Refresh System



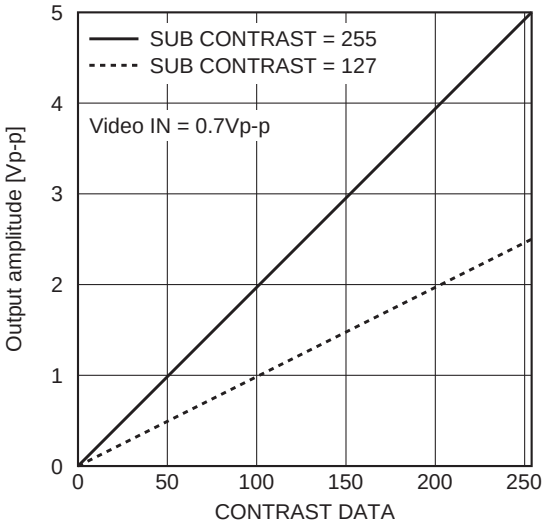
Application Circuit



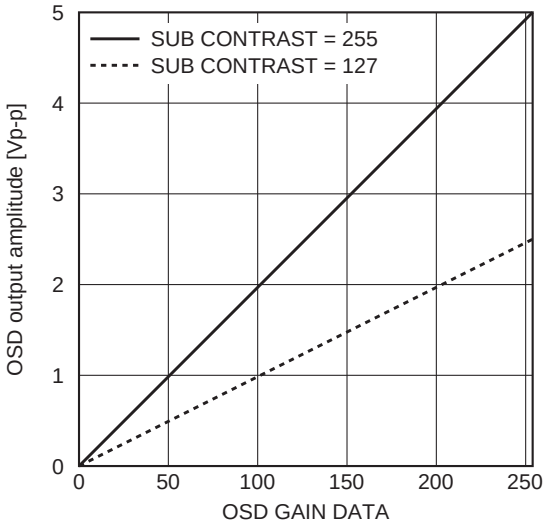
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

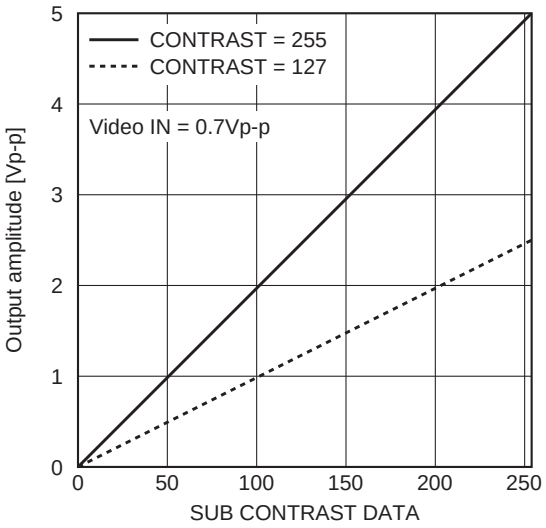
CONTRAST Control Characteristics



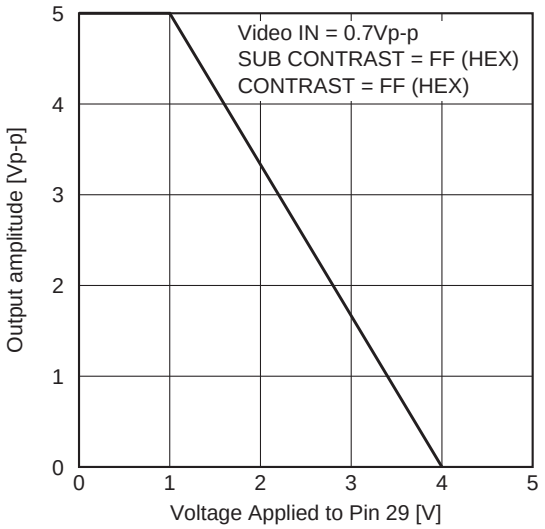
OSD Gain Control Characteristics



SUBCONT Control Characteristics



ABL Control Characteristics

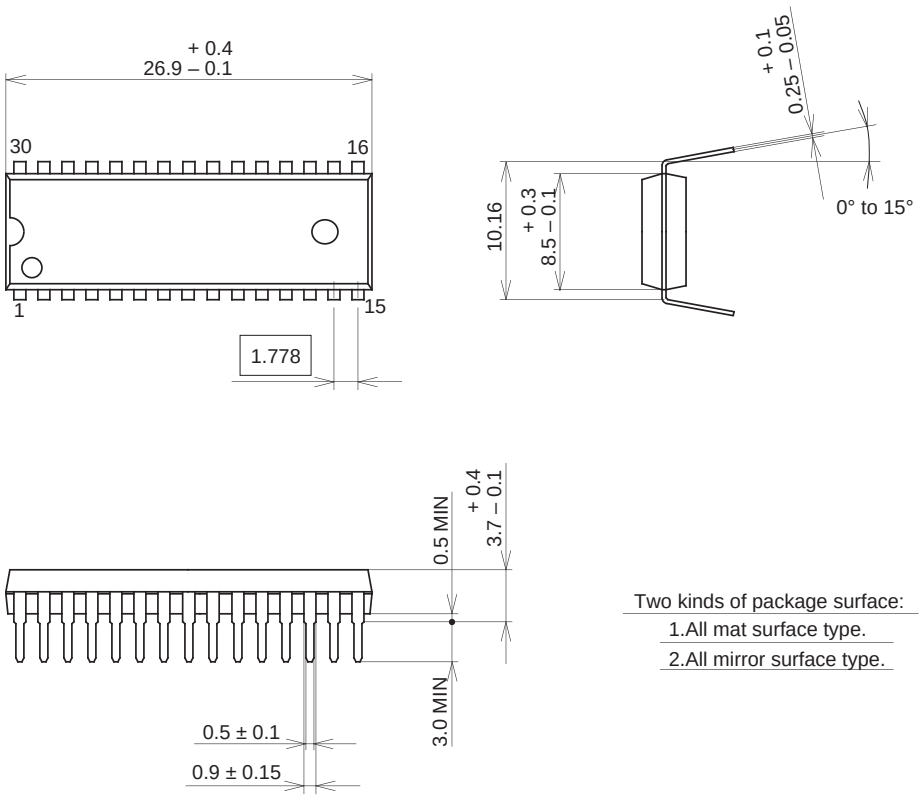


Notes on Operation

1. Set the output for ROUT, GOUT, and BOUT for reception at high impedance.
2. Make the wiring from ROUT, GOUT, and BOUT to the power amplifier as short as possible.
3. Connect the V_{CC} and $V_{CC}2$ decoupling capacitor so that the ceramic capacitor and electrolytic capacitor are connected in parallel and the distance from the IC is as short as possible.
4. Connect the clamp capacitor for RIN, GIN, BIN, S/H-R, S/H-G, S/H-B so that the distance from the IC is as short as possible.
5. Set the output to OFF when the VDET output is not used (Set I^2C BUS VDETOFF "1").

Package Outline Unit: mm

30PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

SONY CODE	SDIP-30P-01
EIAJ CODE	SDIP030-P-0400
JEDEC CODE	————

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).